

Search History

STN
(HCAPLUS, INSPEC, JAPIO, USPATFULL)
2/9/05

=> d his

(FILE 'HOME' ENTERED AT 08:41:15 ON 09 FEB 2005)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 08:41:29 ON
09 FEB 2005

L1 56301 S (GAN OR GALLIUM(W)NITRIDE)
L2 566 S (NITRIDE) (8A) (SEMICONDUCTOR(4A)CHIP#)
L3 2941 S (GROW? OR PRODUC? OR CREAT?) (8A) (NITRIDE(4A)CRYSTAL#)
L4 2821 S (HEXAGONAL) (8A) (SUBSTRATE#)
L5 156 S (CUT?) (8A) (BACK(4A)SURFACE(10A)SUBSTRATE)
L6 197 S (GRIND?) (10A) (BACK(4A)SURFACE(10A)SUBSTRATE)
L7 1087 S (SCRATCH? OR SCRAP?) (8A) (FRONT(6A)SURFACE OR BACK(6A)SURFACE)
L8 3629 S (RHOMBUS)
L9 19827 S (SAPPHIRE(8A)SUBSTRATE)
L10 2 S L1 AND L4 AND L5
L11 5 S L1 AND L4 AND L6

=> s l1 and l4 and l5 and l6 and l7 and l8 and l9
1 FILES SEARCHED...

L12 1 L1 AND L4 AND L5 AND L6 AND L7 AND L8 AND L9

=> d l12 abs,bib

L12 ANSWER 1 OF 1 USPATFULL on STN

AB A method for manufacturing a nitride semiconductor device in which nitride crystals are sequentially grown on a **substrate** such as **sapphire** by MOCVD or the like, and p electrode and n electrode are formed. The wafer is not cut along two perpendicular directions, but rather is cut along two directions that form a 120 degree angle, to obtain a **rhombus** shaped semiconductor chip. Because the wafer has a six-fold rotation symmetry, by cutting the wafer at an angle of 120 degrees, the cutting directions are equivalent and the wafer can be cut in directions along which it can be easily split.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:232645 USPATFULL

TI Nitride semiconductor chip and method for manufacturing nitride semiconductor chip

IN Sakai, Shiro, Tokushima-shi, JAPAN
Lacroix, Yves, Tokushima-shi, JAPAN

PI US 2002124794 A1 20020912

AI US 2002-44686 A1 20020111 (10)

PRAI JP 2001-3910 20010111

DT Utility

FS APPLICATION

LREP ROSENTHAL & OSHA L.L.P., 1221 MCKINNEY AVENUE, SUITE 2800, HOUSTON, TX,
77010

CLMN Number of Claims: 11

ECL Exemplary Claim: 1

DRWN 4 Drawing Page(s)

LN.CNT 293

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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Search History

=> d 111 1-5 abs,bib

L11 ANSWER 1 OF 5 USPATFULL on STN

AB An image display unit and a method of producing the image display unit, wherein the image display unit includes an array of a plurality of light emitting devices for displaying an image, and wherein the method of producing the image display unit employs, for example, a space expanding transfer, whereby a first transfer step includes transferring the devices arrayed on a first substrate to a temporary holding member such that the devices are spaced from each other with a pitch larger than a pitch of the devices arrayed on the first substrate, a second holding step includes holding the devices on the temporary holding member, and a third transfer step includes transferring the devices held on the temporary holding member onto a second board such that the devices are spaced from each other with a pitch larger than the pitch of the devices held on the temporary holding member.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2004:151628 USPATFULL

TI Image display unit and method of producing image display unit

IN Iwafuchi, Toshiaki, Kanagawa, JAPAN

Oohata, Toyoharu, Kanagawa, JAPAN

Doi, Masato, Kanagawa, JAPAN

PI US 2004115849 A1 20040617

AI US 2003-427815 A1 20030430 (10)

RLI Division of Ser. No. US 2002-66423, filed on 30 Jan 2002, GRANTED, Pat. No. US 6613610 Continuation of Ser. No. WO 2001-JP6213, filed on 18 Jul 2001, UNKNOWN

PRAI JP 2000-217953 20000718

JP 2000-217988 20000718

JP 2000-396225 20001226

JP 2001-200113 20010629

DT Utility

FS APPLICATION

LREP BELL, BOYD & LLOYD LLC, P.O. Box 1135, Chicago, IL, 60690

CLMN Number of Claims: 54

ECL Exemplary Claim: 1

DRWN 40 Drawing Page(s)

LN.CNT 3105

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L11 ANSWER 2 OF 5 USPATFULL on STN

AB A display unit and semiconductor light emitting devices are provided. The display unit includes a number of the semiconductor light emitting devices arrayed on a base body, wherein each of the semiconductor light emitting devices is formed together with dummy devices for setting an emission wavelength of the semiconductor light emitting device, and the semiconductor light emitting device is formed by selective growth, and one conductive layer is formed in self-alignment on planes grown from tilt planes formed by selective growth. Such a display unit has a structure suitable for multi-colors without increasing the number of production steps.

AN 2002:305992 USPATFULL

TI Display unit and semiconductor light emitting device

IN Okuyama, Hiroyuki, Kanagawa, JAPAN

Doi, Masato, Kanagawa, JAPAN

Biwa, Goshi, Kanagawa, JAPAN

Oohata, Toyoharu, Kanagawa, JAPAN

Minami, Masaru, Kanagawa, JAPAN

PI US 2002171089 A1 20021121

AI US 2002-92687 A1 20020306 (10)

PRAI JP 2001-62206 20010306

JP 2001-362444 20011128
DT Utility
FS APPLICATION
LREP Bell, Boyd & Lloyd LLC, P.O. Box 1135, Chicago, IL, 60690
CLMN Number of Claims: 26
ECL Exemplary Claim: 1
DRWN 28 Drawing Page(s)
LN.CNT 2612

L11 ANSWER 3 OF 5 USPATFULL on STN

AB A method for manufacturing a nitride semiconductor device in which nitride crystals are sequentially grown on a substrate such as sapphire by MOCVD or the like, and p electrode and n electrode are formed. The wafer is not cut along two perpendicular directions, but rather is cut along two directions that form a 120 degree angle, to obtain a rhombus shaped semiconductor chip. Because the wafer has a six-fold rotation symmetry, by cutting the wafer at an angle of 120 degrees, the cutting directions are equivalent and the wafer can be cut in directions along which it can be easily split.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:232645 USPATFULL
TI Nitride semiconductor chip and method for manufacturing nitride semiconductor chip
IN Sakai, Shiro, Tokushima-shi, JAPAN
Lacroix, Yves, Tokushima-shi, JAPAN
PI US 2002124794 A1 20020912
AI US 2002-44686 A1 20020111 (10)
PRAI JP 2001-3910 20010111
DT Utility
FS APPLICATION
LREP ROSENTHAL & OSHA L.L.P., 1221 MCKINNEY AVENUE, SUITE 2800, HOUSTON, TX, 77010
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 4 Drawing Page(s)
LN.CNT 293

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L11 ANSWER 4 OF 5 USPATFULL on STN

AB An image display unit and a method of producing the image display unit, wherein the image display unit includes an array of a plurality of light emitting devices for displaying an image, and wherein the method of producing the image display unit employs, for example, a space expanding transfer, whereby a first transfer step includes transferring the devices arrayed on a first substrate to a temporary holding member such that the devices are spaced from each other with a pitch larger than a pitch of the devices arrayed on the first substrate, a second holding step includes holding the devices on the temporary holding member, and a third transfer step includes transferring the devices held on the temporary holding member onto a second board such that the devices are spaced from each other with a pitch larger than the pitch of the devices held on the temporary holding member.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:184106 USPATFULL
TI Image display unit and method of producing image display unit
IN Iwafuchi, Toshiaki, Kanagawa, JAPAN
Oohata, Toyoharu, Kanagawa, JAPAN
Doi, Masato, Kanagawa, JAPAN
PI US 2002096994 A1 20020725
US 6613610 B2 20030902
AI US 2002-66423 A1 20020130 (10)

RLI Continuation of Ser. No. WO 2001-JP6213, filed on 18 Jul 2001, UNKNOWN
PRAI JP 2000-217953 20000718
JP 2000-217988 20000718
JP 2000-396225 20001226
JP 2001-200113 20010629
DT Utility
FS APPLICATION
LREP BELL, BOYD & LLOYD, LLC, P. O. BOX 1135, CHICAGO, IL, 60690-1135
CLMN Number of Claims: 54
ECL Exemplary Claim: 1
DRWN 41 Drawing Page(s)
LN.CNT 3108
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L11 ANSWER 5 OF 5 USPAT2 on STN
AB An image display unit and a method of producing the image display unit,
wherein the image display unit includes an array of a plurality of light
emitting devices for displaying an image, and wherein the method of
producing the image display unit employs, for example, a space expanding
transfer, whereby a first transfer step includes transferring the
devices arrayed on a first substrate to a temporary holding member such
that the devices are spaced from each other with a pitch larger than a
pitch of the devices arrayed on the first substrate, a second holding
step includes holding the devices on the temporary holding member, and a
third transfer step includes transferring the devices held on the
temporary holding member onto a second board such that the devices are
spaced from each other with a pitch larger than the pitch of the devices
held on the temporary holding member.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:184106 USPAT2
TI Image display unit and method of producing image display unit
IN Iwafuchi, Toshiaki, Kanagawa, JAPAN
Oohata, Toyoharu, Kanagawa, JAPAN
Doi, Masato, Kanagawa, JAPAN
PA Sony Corporation, Tokyo, JAPAN (non-U.S. corporation)
PI US 6613610 B2 20030902
AI US 2002-66423 20020130 (10)
RLI Continuation of Ser. No. WO 2001-JP6213, filed on 18 Jul 2001
PRAI JP 2000-217953 20000718
JP 2000-217988 20000718
JP 2000-396225 20001226
JP 2001-200113 20010629
DT Utility
FS GRANTED
EXNAM Primary Examiner: Dang, Trung
LREP Bell, Boyd & Lloyd LLC
CLMN Number of Claims: 20
ECL Exemplary Claim: 1
DRWN 68 Drawing Figure(s); 41 Drawing Page(s)
LN.CNT 2886
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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(FILE 'HOME' ENTERED AT 08:41:15 ON 09 FEB 2005)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 08:41:29 ON
09 FEB 2005

L1 56301 S (GAN OR GALLIUM(W)NITRIDE)
L2 566 S (NITRIDE) (8A) (SEMICONDUCTOR(4A)CHIP#)
L3 2941 S (GROW? OR PRODUC? OR CREAT?) (8A) (NITRIDE(4A)CRYSTAL#)

L4 2821 S (HEXAGONAL) (8A) (SUBSTRATE#)
L5 156 S (CUT?) (8A) (BACK(4A) SURFACE(10A) SUBSTRATE)
L6 197 S (GRIND?) (10A) (BACK(4A) SURFACE(10A) SUBSTRATE)
L7 1087 S (SCRATCH? OR SCRAP?) (8A) (FRONT(6A) SURFACE OR BACK(6A) SURFACE)
L8 3629 S (RHOMBUS)
L9 19827 S (SAPPHIRE(8A) SUBSTRATE)
L10 2 S L1 AND L4 AND L5
L11 5 S L1 AND L4 AND L6

=>

Search History

=> d 110 1-2 abs,bib

L10 ANSWER 1 OF 2 USPATFULL on STN

AB A method for manufacturing a nitride semiconductor device in which nitride crystals are sequentially grown on a substrate such as sapphire by MOCVD or the like, and p electrode and n electrode are formed. The wafer is not cut along two perpendicular directions, but rather is cut along two directions that form a 120 degree angle, to obtain a rhombus shaped semiconductor chip. Because the wafer has a six-fold rotation symmetry, by cutting the wafer at an angle of 120 degrees, the cutting directions are equivalent and the wafer can be cut in directions along which it can be easily split.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:232645 USPATFULL

TI Nitride semiconductor chip and method for manufacturing nitride semiconductor chip

IN Sakai, Shiro, Tokushima-shi, JAPAN

Lacroix, Yves, Tokushima-shi, JAPAN

PI US 2002124794 AI 20020912

AI US 2002-44686 AI 20020111 (10)

PRAI JP 2001-3910 20010111

DT Utility

FS APPLICATION

LREP ROSENTHAL & OSHA L.L.P., 1221 MCKINNEY AVENUE, SUITE 2800, HOUSTON, TX, 77010

CLMN Number of Claims: 11

ECL Exemplary Claim: 1

DRWN 4 Drawing Page(s)

LN.CNT 293

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L10 ANSWER 2 OF 2 USPATFULL on STN

AB A wedge-like etching groove is formed so that stresses can be collected along a cleavage surface of a nitride based compound semiconductor, and end portions are separated from a substrate. With these operations, a light-emitting layer can form an excellent mirror by a natural cleavage. Further, by separating a portion of the end surfaces from the substrate, it is possible to suppress a deformation from the substrate and therefore, a deterioration due to the deformation can be prevented. Therefore, it is possible to provide a nitride based compound semiconductor light-emitting device which can form an excellent cleavage surface with a simple process.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 1999:132618 USPATFULL

TI Nitride based compound semiconductor light emitting device and method for producing the same

IN Saito, Shinji, Yokohama, Japan

Rennie, John, Bunkyo-ku, Japan

Onomura, Masaaki, Kawasaki, Japan

Hatakoshi, Genichi, Yokohama, Japan

PA Kabushiki Kaisha Toshiba, Kawasaki, Japan (non-U.S. corporation)

PI US 5972730 19991026

AI US 1997-937160 19970925 (8)

PRAI JP 1996-254960 19960926

DT Utility

FS Granted

EXNAM Primary Examiner: Dutton, Brian

LREP Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

CLMN Number of Claims: 12

ECL Exemplary Claim: 1

DRWN 22 Drawing Figure(s); 16 Drawing Page(s)

LN.CNT 985
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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(FILE 'HOME' ENTERED AT 08:41:15 ON 09 FEB 2005)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 08:41:29 ON
09 FEB 2005

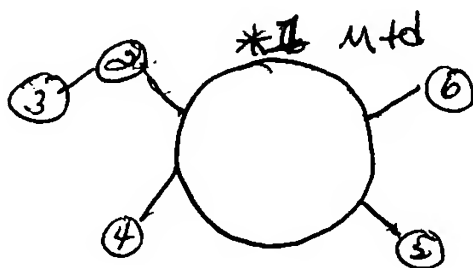
L1	56301	S	(GAN OR GALLIUM(W)NITRIDE)
L2	566	S	(NITRIDE) (8A) (SEMICONDUCTOR(4A)CHIP#)
L3	2941	S	(GROW? OR PRODUC? OR CREAT?) (8A) (NITRIDE(4A)CRYSTAL#)
L4	2821	S	(HEXAGONAL) (8A) (SUBSTRATE#)
L5	156	S	(CUT?) (8A) (BACK(4A)SURFACE(10A)SUBSTRATE)
L6	197	S	(GRIND?) (10A) (BACK(4A)SURFACE(10A)SUBSTRATE)
L7	1087	S	(SCRATCH? OR SCRAP?) (8A) (FRONT(6A)SURFACE OR BACK(6A)SURFACE)
L8	3629	S	(RHOMBUS)
L9	19827	S	(SAPPHIRE(8A)SUBSTRATE)
L10	2	S	L1 AND L4 AND L5
L11	5	S	L1 AND L4 AND L6

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10/092,231
 10/184,305
 10/102,863

Examiner's Notes

S (GaN or gallium(N) Nitride)
 S (Nitride) (8a) (semiconductor (4a) chip)
 S (grow? or produce? or create?) (8a) (Nitride (4a) crystal #)
 S (hexagonal) (10a) (substrate)
 S (cut?) (10a) back (4a) surface (10a) substrate
 S (grind?) (10a) (back (4a) surface (10a) substrate)
 S (scratch?) (8a) (front (10a) surface or back (6a) surface)
 S (rhombus)
 S (sapphire (8a) substrate)



Motivation: In order to produce & efficiently form a nitride semiconductor chip composed of uniform crystal grains in a large area.

(EP 0 967 328 A2 reference)

MotoKi teaches a method of producing a GaN ~~type~~ semiconductor device comprising ~~"GaN" or gallium nitride single crystal substrates~~ using sapphire substrates (col. 1, lines 1-18). Sapphire is a suitable material for the substrate of the epitaxial growth at a high temperature due to its properties (i.e. high stability, high rigidity & high heat-resistance). GaN single crystal layers are grown alone on a sapphire substrate to create a light emitting device. A silicon or a GaAs substrate is also used since it has natural cleavage planes in the direction perpendicular to each other, a wafer is easily diced up into individual chips along two groups of parallel lines being at right angles to each other (col. 1, lines 28-38; col. 2, lines 1-5). ~~The sapphire~~ The sapphire is forced into cutting with a mechanical (i.e. rolling plate) cutter, since it has no cleavage planes.